

U.S. Patent Application Serial No. 10/665,204
Response filed September 18, 2006
Reply to OA dated May 22, 2006

REMARKS

Claims 1 - 16 and 22 are canceled, without prejudice or disclaimer, in this patent application.

Claims 17, 20 and 23 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated May 22, 2006.

Claims 17 - 21 and 23 remain in this patent application, claims 17 and 23 being independent claims.

At the outset, the applicants thank the Examiner withdrawing his previous objections to the specification and claims found in the previous Office Action in view of the applicants' amendments of February 21, 2006.

However, the drawings are objected to as the Examiner alleges that the drawings do not show every feature of the invention specified in the claims. Therefore, a semiconductor optical waveguide path (claim 22) must be shown or the feature canceled from the claim.

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The applicants have canceled claim 22 without prejudice or disclaimer, the objection to the drawings stemming from claim 22. Thus, the outstanding objection to the drawings is now moot.

In view of the above, the withdrawal of the outstanding objection to the drawings is in order, and is therefore respectfully solicited.

Claim 20 is rejected under 35 USC §112, first paragraph. The Examiner alleges that claim 20 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention.

The Examiner alleges that the specification merely discloses (see, page 8, lines 29 - 35) that a predetermined potential is supplied to each of the n-side and p-side electrodes, and according to the Examiner, there is no discussion in the applicants' specification about a predetermined potential being supplied to the contact layer or that the n-side and p-side electrodes have a high impurity concentration.

The applicants respectfully request reconsideration of this rejection.

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First, claim 20 recites that the contact layer has a high impurity concentration, not n-side and p-side electrodes, as alleged by the Examiner. At, e.g, page 7, lines 10-11 of the applicants' specification, such high impurity concentration is disclosed for contact layer (12).

Second, although it is not specifically disclosed that a predetermined potential is supplied to the contact layer (12), one of ordinary skill in the art would recognize that if a predetermined potential is supplied to an electrode (such as element 21 in the applicants' Figure 2) in a contact layer (such as element 12 in the applicants' Figure 2), then the predetermined potential is supplied to that contact layer.

In addition to the applicants' above remarks, the applicants have amended claim 20 so as to recite "...a predetermined potential being supplied to the contact layer through an electrode connected to the contact layer." The applicants' Figure 2 and the text of page 8, lines 29 - 35, wherein it is disclosed that a predetermined potential is supplied to the n-side electrode 21, provide a basis for the amendments to claim 20. Further, claim 20 is supported by the description in lines 22 - 30, page 7 of the applicants' specification.

In view of the above, the withdrawal of the outstanding 35 USC §112, first paragraph, rejection is in order, and is therefore respectfully solicited.

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As to the merits of this case, first, claim 14 stands rejected under 35 USC §103(a) as being unpatentable over the “admitted prior art” (APA) in view of Takahashi (JP 59-161082) and Fujimura (U.S. Patent Publication No. 2002/0149827). The Examiner alleges that APA discloses the claimed device, except for the intermediate layer and the light receiving surface on the bottom surface of the substrate. The Examiner further alleges that Takahashi discloses the intermediate layer and that Fujimura discloses the light receiving surface.

The applicants respectfully request reconsideration of this rejection.

As indicated above, claim 14 has been canceled without prejudice or disclaimer. Thus, the outstanding rejection of claim 14 is now moot.

Accordingly, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on APA in view of Takahashi (JP 59-161082) and Fujimura (U.S. Patent Publication No. 2002/0149827) is in order, and is therefore respectfully solicited.

Second, claims 17 - 19, 21 and 22 are rejected under 35 USC §103(a) as being unpatentable over Ajisawa (U.S. Patent No. 5,825,047) in view of Vilela (U.S. Patent No. 5,800,630).

The Examiner alleges that Ajisawa discloses the claimed semiconductor light-receiving device, except for a semiconductor layer of a first conduction type that is formed on the semi-insulating substrate and a semiconductor intermediate layer having a higher impurity concentration than a buffer layer. The Examiner further alleges that Vilela discloses those components, as shown in Figure 4 at a bottom layer and a third layer from the bottom, respectively. The applicants respectfully request reconsideration of this rejection.

At the outset, the applicants submit that there is no motivation to combine the teachings of Vilela and Ajisawa in the manner suggested by the Examiner. Vilela relates to a solar cell, and particularly intends to improve the power efficiency by vertically stacking multiple solar cells having different light-receiving wavelengths. Vilela's device employs InP and InGaAs, which are also used in the present invention. However, Vilela discloses nothing other than solar cells that generates electrical power, and nothing about high-speed signal processing.

Ajisawa relates to a light-receiving device that converts an optical high-speed signal into an electrical high-speed signal, and thus relates to the technical field quite different from that of Vilela. Ajisawa utilizes the electric field formed within the device externally supplied with a voltage and moves the electrons and holes generated in the light absorption layer towards the two electrodes. In contrast, Vilela teaches a device in which a voltage (electric field) is generated between the two electrodes by irradiation of light. Thus, the functions and operations of Vilela's device are quite

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different from those of Ajisawa's device, and there is no motivation to combine the teachings of Vilela with the teachings of Ajisawa.

Moreover, Figure 4 of Vilela is "a device grown in the laboratory to measure the peak current of the tunnel junction of this invention." Although the third layer from the bottom is a tunnel junction, it is a tunnel junction shown being measured in a measuring device for use in a tandem solar cell, not in a semiconductor light-receiving device (photodiode), as in the applicants' present invention. Vilela does not disclose or suggest arranging such a tunnel junction between a buffer layer and a light absorption layer of a semiconductor light-receiving device, as presently claimed, or between similar layers in a solar cell.

It is thus respectfully submitted that the cited tunnel junction has been taken completely out of context in the outstanding Office Action in order to allege that Vilela discloses or suggests the present claimed invention.

In view of the above, a person of ordinary skill in the art would not have combined the teachings of Ajisawa and Vilela because there would have been no motivation for doing so; and even if *arguendo* the teachings of Ajisawa and Vilela are combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meting the applicants' claimed invention.

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In view of the above, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Ajisawa (U.S. Patent No. 5,825,047) in view of Vilela (U.S. Patent No. 5,800,630) is in order, and is therefore respectfully solicited.

Third, claim 23 is rejected under 35 USC § 103(a) as being unpatentable over Watanabe (JP 6-90016) in view of Vilela.

The Examiner alleges that Watanabe discloses the claimed invention, except for the intermediate tunneling layer having a higher impurity concentration than the buffer layer. The Examiner again alleges that Vilela discloses such intermediate layer. The applicants respectfully request reconsideration of this rejection.

As discussed above, the Examiner has taken the tunneling layer of Vilela out of context to allege that Vilela teaches using such a tunneling layer in a semiconductor light-receiving device of the present claimed invention. The applicants traverse the Examiner's position on this point for the reasons more particularly discussed above.

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Accordingly, even if *arguendo* the teachings of Watanabe and Vilela are combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meting the applicants' claimed invention, as now recited in claim 23. Thus, a person of ordinary skill in the art would not have found the applicants' claimed invention, as now set forth in claim 23, obvious based on the teachings of Watanabe and Vilela, singly or in combination.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 USC § 103(a) based on Watanabe (JP 6-90016) in view of Vilela is in order, and is therefore respectfully solicited.

Furthermore, in paragraph 12 of the Office Action, the Examiner states that in response to the argument that Vilela is not a light-receiving device, the claim language "...light-receiving device" has not been given patentable weight because the recitation occurs in the preamble. In response, the applicants have amended each of claims 14, 17 and 23 so as to more particularly recite in the body of each of these claims that the claimed substrate and layers are arranged to form a semiconductor light-receiving device.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

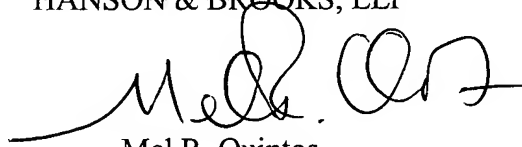
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If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview in order to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosure: Petition for Extension of Time